REMARKS/ARGUMENTS

With respect to the objection to the specification, Applicant respectfully notes that the instances of omitted periods set forth in the Office Action cannot be found. Applicant respectfully requests further explanation of this objection.

Claim 5 has been amended to overcome the claim objection thereto.

Pending claims 1-4, 6, 8-11, 16 and 18-24 stand rejected under 35 U.S.C. §102(e) over U.S. Publication Number 2002/0031166 (Subramanian). Applicant respectfully traverses the rejection. As to claim 1, Subramanian does not disclose, at least, a reconfigurable logic core coupled to receive a digitized RF signal from an analog-to-digital converter (ADC). In this regard, the Office Action contends that DSP/microprocessor 112 of Subramanian is the recited reconfigurable logic core. However, note that this component 112 is not coupled to receive digitized data from an ADC. Furthermore, Subramanian nowhere teaches a plurality of general-purpose processor cores coupled to the reconfigurable logic core. In this regard, the Office Action contends that modem processor 102 and codec processor 104 are the recited general-purpose processors. However, as Subramanian clearly teaches, these components are not general-purpose processors, but instead specific modem and codec processors: "functions....are performed by the present invention on operation-specific, or algorithm-specific, processors that are interconnected to realize a modem or codec function." Subramanian, ¶ 49. For at least these reasons, claim 1 and the claims depending therefrom are patentable over Subramanian.

Independent claim 11 is patentable for at least similar reasons as Subramanian does not teach a reconfigurable logic core coupled to receive converted data from an ADC. Instead, as described above the DSP/microprocessor 112 of Subramanian is not coupled to receive data from an ADC. Further, as described with regard to claim 1 Subramanian does not include a plurality of general-purpose processor cores coupled to a reconfigurable logic core. For at least these reasons, claim 11 and the claims depending therefrom are patentable over Subramanian.

Dependent claim 2 is further patentable, as Subramanian nowhere teaches that its device can handle a short-range wireless protocol, as recited by claim 2.

Dependent claim 8 is further patentable, as Subramanian nowhere teaches a router that routes packets to a cellular radio core and a short-range wireless transceiver core. In this regard, the Office Action contends that the recited router is met by an allocator that provides data to planes of a modem processor. Nowhere, however, does Subramanian teach that this allocator

routes packets to both a cellular radio core and a short-range wireless transceiver core. Clearly, the modem of Subramanian is not part of any radio (i.e., RF) cores. For at least the same reasons dependent claims 9 and 10 are patentable. Furthermore, Subramanian nowhere teaches sending packets in parallel via multiple wireless transmission media, as recited by claims 9 and 10. For at least similar reasons, dependent claims 18-20 are also patentable.

Dependent claim 22 is further patentable as Subramanian nowhere teaches presence of a vector processor. In this regard, the Office Action merely refers to DSP/microprocessor 112. However, Subramanian nowhere teaches that this component is a vector processor. For this further reason, dependent claim 22 is patentable.

Pending claims 5, 7 and 17 stand rejected under 35 U.S.C. §103(a) over Subramanian in view of U.S. Patent Number 6,096,091 (Hartmann). Applicant respectfully traverses the rejection. As to claim 5, the Office Action concedes that Subramanian does not teach presence of a FIFO memory. Office Action, page 8. Applicant respectfully disagrees that Subramanian teaches "a memory positioned between the reconfigurable logic core and at least one of the one or more general-purpose processor cores....." Office Action, page 8. Further, memory 106 is not "positioned between processor 112 and processor 102a" as contended by the Office Action. Instead, memory 106 is coupled between modem processor 102 and channel codec processor 104. Because these are not general-purpose processor cores (as described above), Subramanian fails to teach the subject matter contended by the Office Action.

Furthermore, Hartmann also fails to teach the subject matter contended by the Office Action. In this regard, buffer 120a of Hartmann is not positioned between reconfigurable logic network 110a and embedded processor 150. Instead, as clearly shown in Hartmann, buffer 120a is coupled between reconfigurable logic networks 110a and 110b. Accordingly, both references fail to teach or suggest the subject matter contended by the Office Action. As the references, either alone or in combination, fail to teach or suggest all claimed subject matter, the rejection is improper. MPEP §2143. Accordingly, the rejection of claim 5 is overcome.

As to dependent claims 7 and 17, there is no motivation to combine the embedded processor of Hartmann into the system of Subramanian. In this regard, Hartmann teaches that the embedded processor is to control reconfiguration of Hartmann's reconfigurable logic networks. Hartmann, col. 4, lns. 47-50. There is no teaching or suggesting in either reference to

combine this embedded processor with the teaching of Subramanian. For this further reason, the rejection of claims 7 and 17 is overcome.

In view of these remarks, the application is now in condition for allowance and the Examiner's prompt action in accordance therewith is respectfully requested. The Commissioner is authorized to charge any additional fees or credit any overpayment to Deposit Account No. 20-1504.

Respectfully submitted,

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